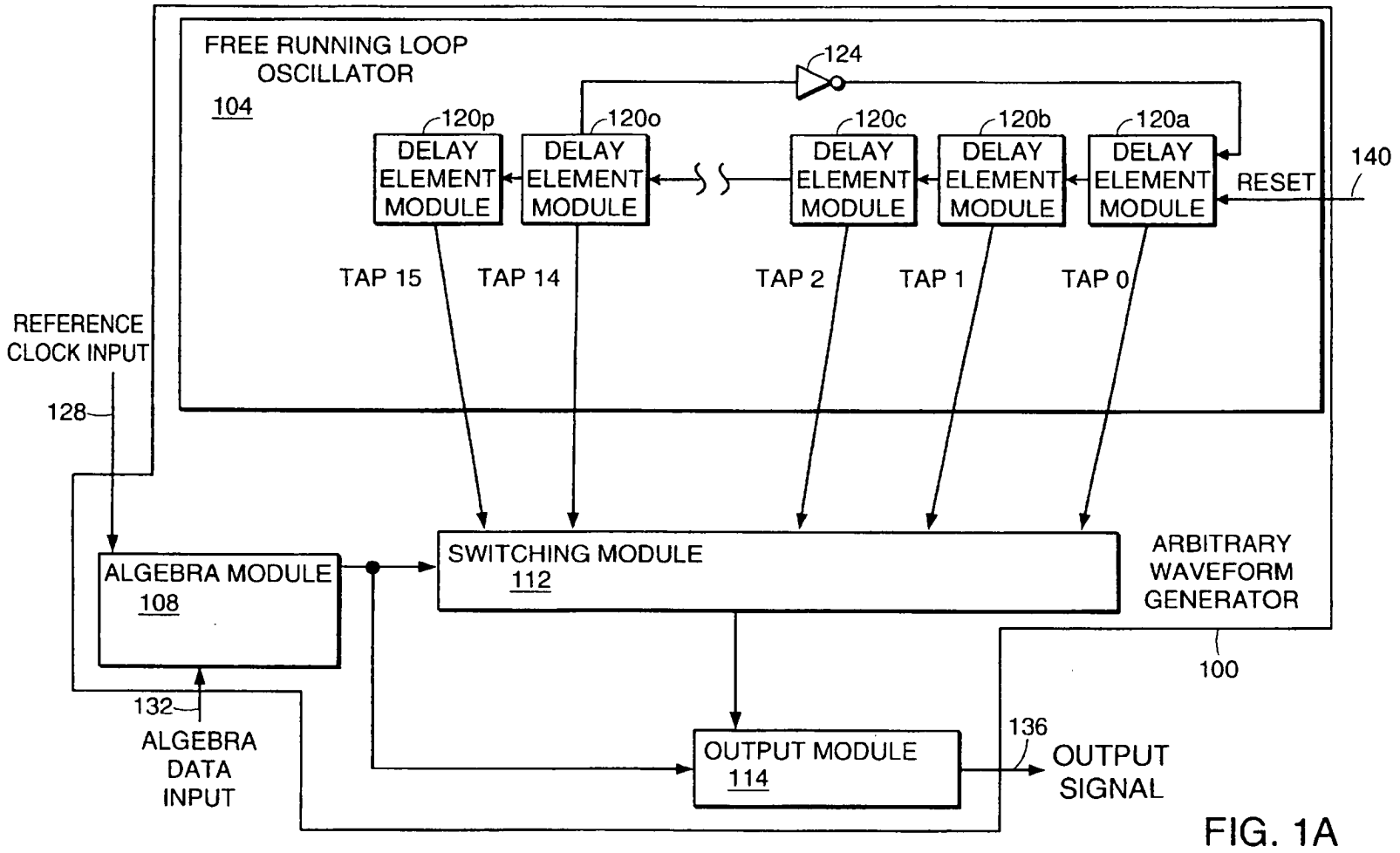

FREE RUNNING LOOP
OSCILLATOR
104
124
120p
120o
120c
120b
120a
DELAY ELEMENT MODULE
DELAY ELEMENT MODULE
DELAY ELEMENT MODULE
DELAY ELEMENT MODULE
DELAY ELEMENT MODULE
RESET
140
TAP 15
TAP 14
TAP 2
TAP 1
TAP 0
REFERENCE CLOCK INPUT
128
ALGEBRA MODULE
108
SWITCHING MODULE
112
ARBITRARY WAVEFORM GENERATOR
100
132
ALGEBRA DATA INPUT
OUTPUT MODULE
114
136
OUTPUT SIGNAL

FIG. 1A

TIMING DIAGRAM - FREE RUNNING OSCILLATOR DELAY OUTPUTS

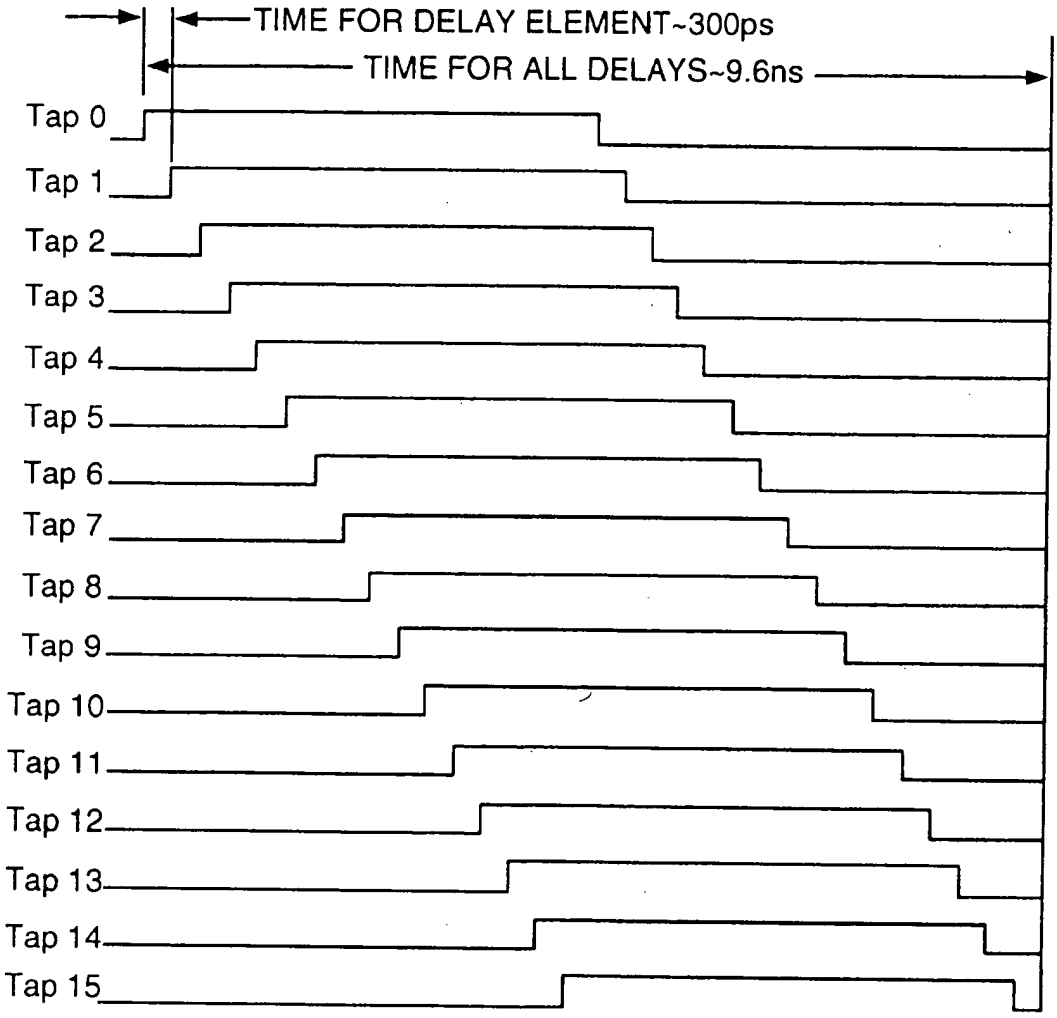


FIG. 1B

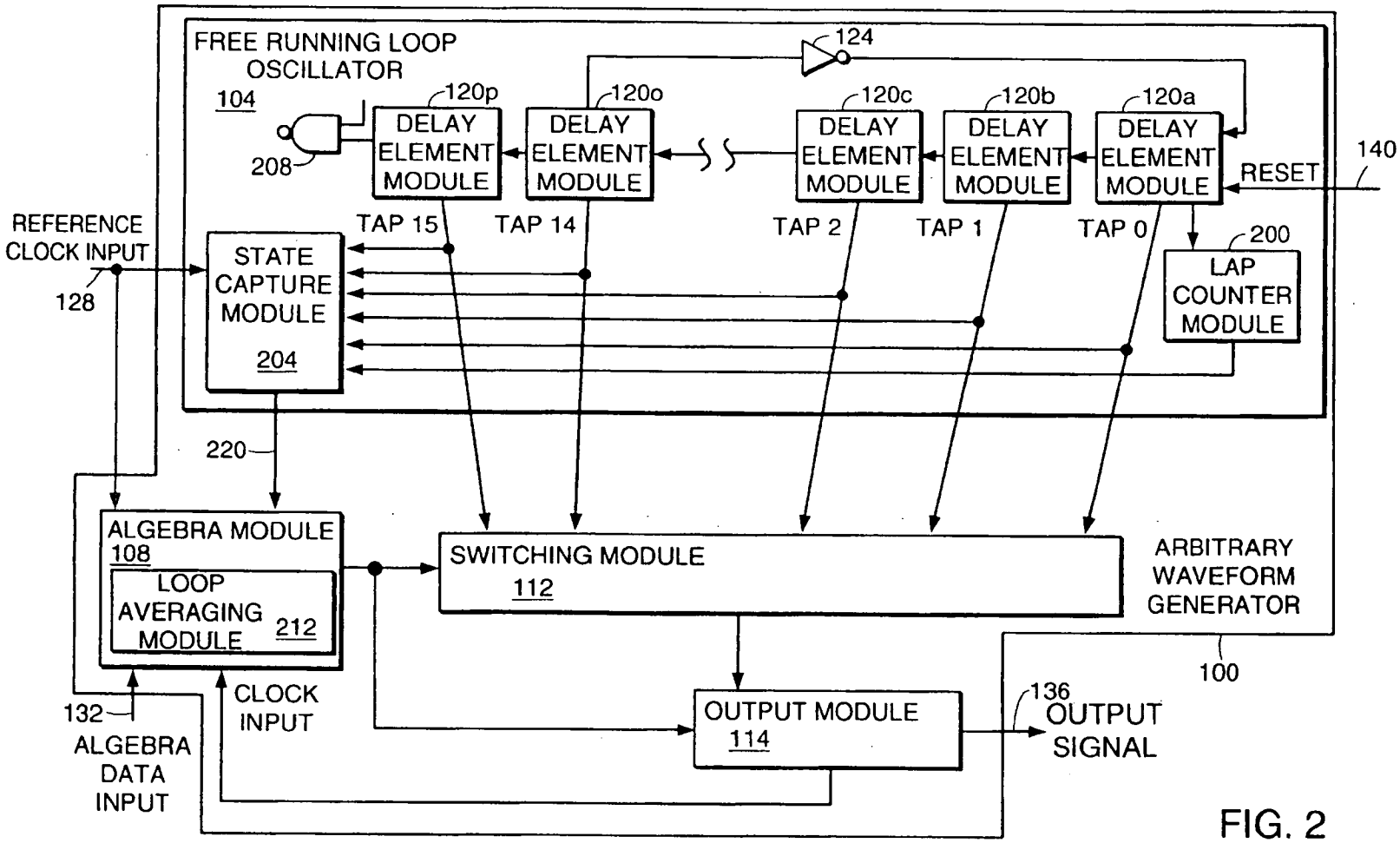

FREE RUNNING LOOP OSCILLATOR
104
124
120p
120o
120c
120b
120a
DELAY ELEMENT MODULE
208
RESET
140
REFERENCE CLOCK INPUT
128
TAP 15
TAP 14
TAP 2
TAP 1
TAP 0
STATE CAPTURE MODULE
204
200
LAP COUNTER MODULE
220
ALGEBRA MODULE
108
LOOP AVERAGING MODULE
212
SWITCHING MODULE
112
ARBITRARY WAVEFORM GENERATOR
100
132
ALGEBRA DATA INPUT
CLOCK INPUT
OUTPUT MODULE
114
136
OUTPUT SIGNAL

FIG. 2

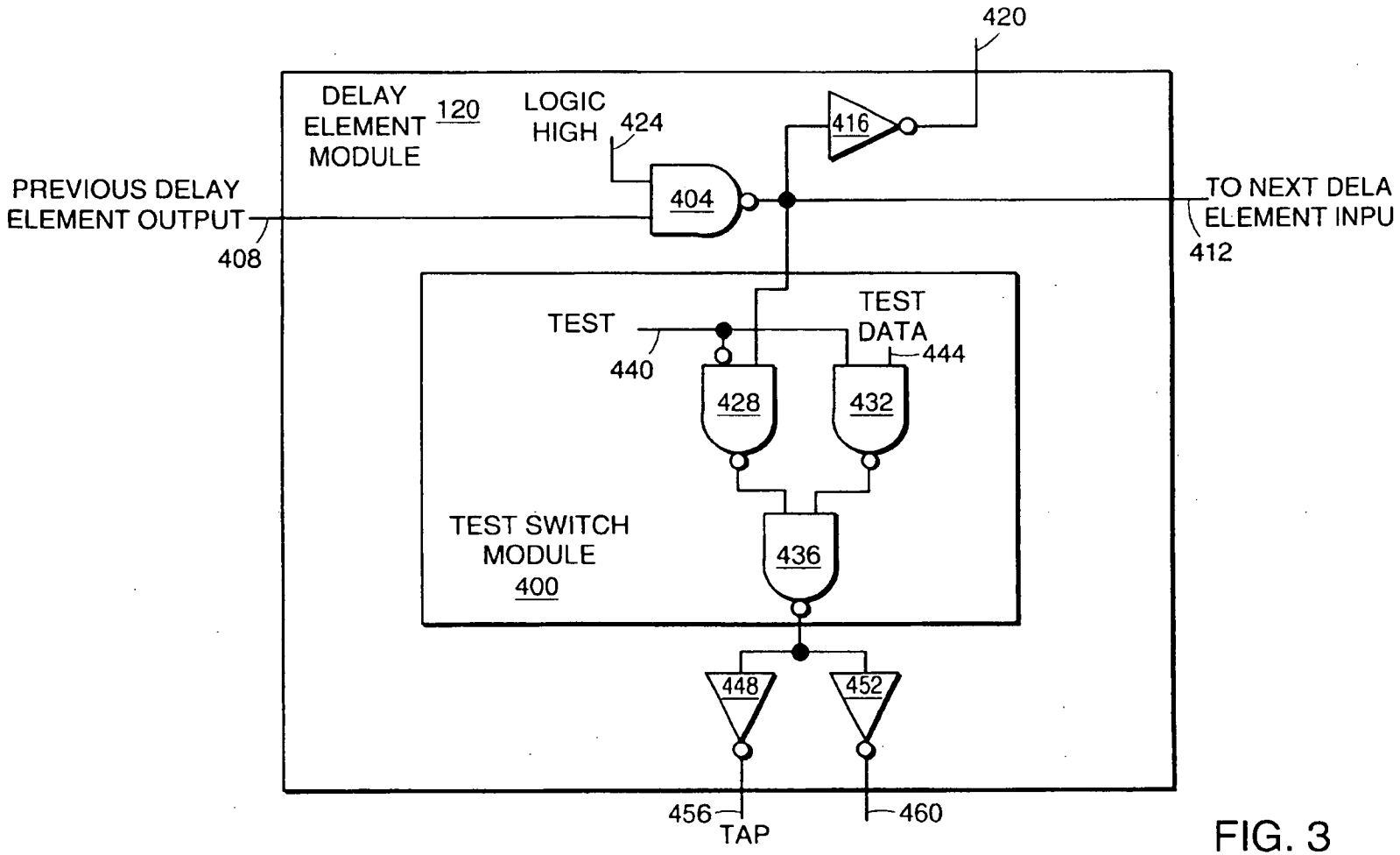

420
DELAY ELEMENT MODULE 120
LOGIC HIGH 424
416
404
PREVIOUS DELAY ELEMENT OUTPUT
408
TO NEXT DELA ELEMENT INPU
412
TEST
440
TEST DATA
444
428
432
TEST SWITCH MODULE 400
436
448
452
456
TAP
460

FIG. 3

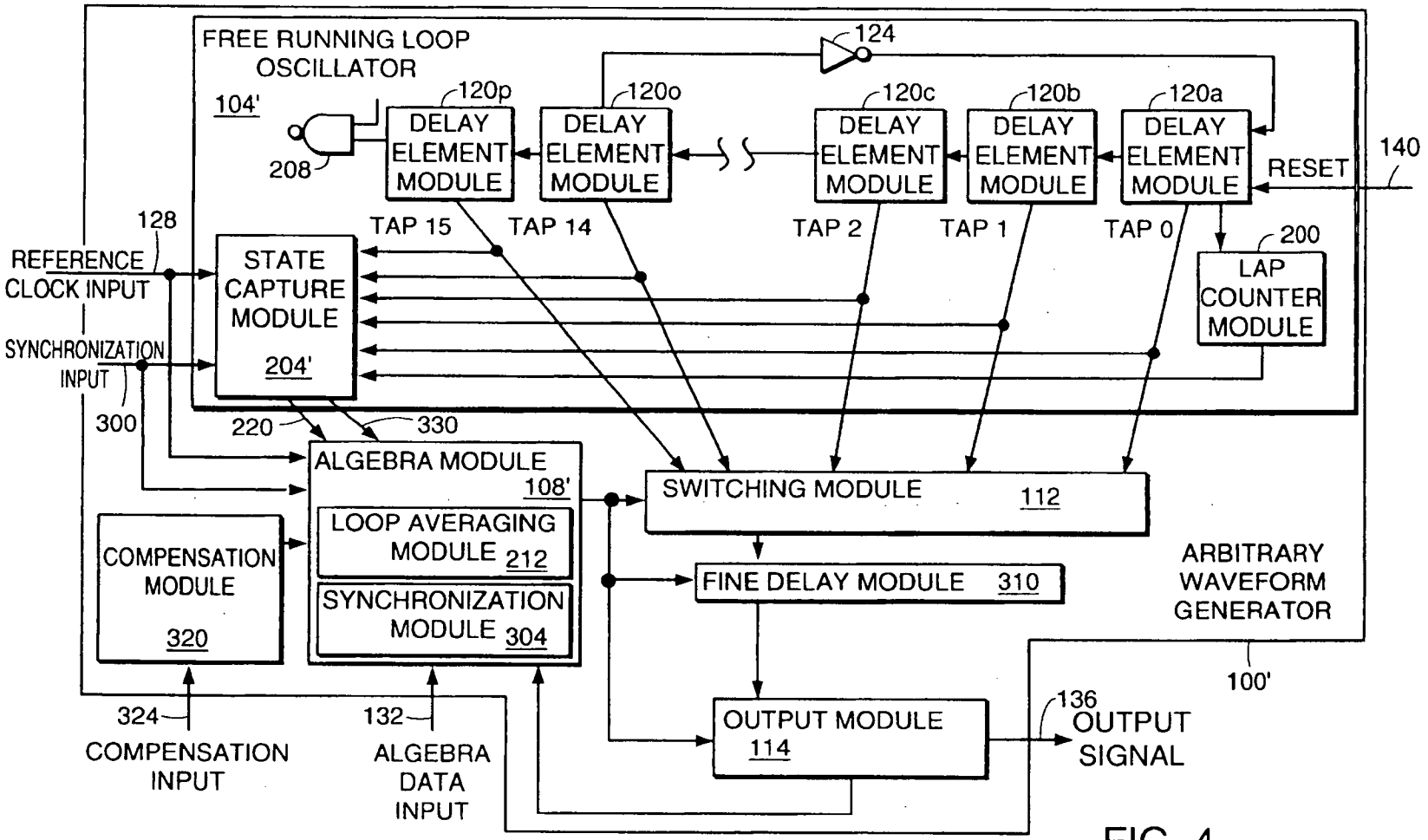
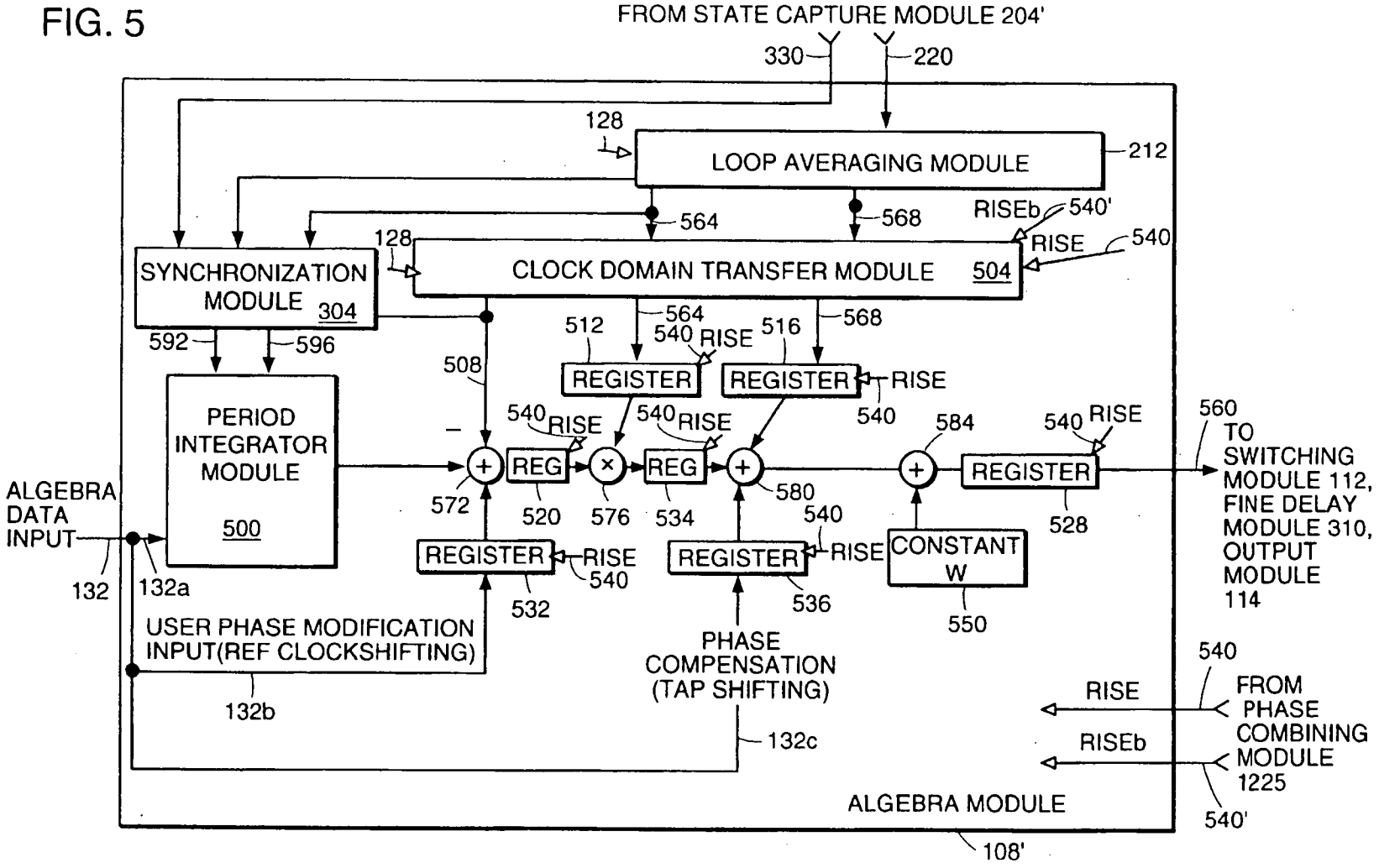

FREE RUNNING LOOP OSCILLATOR
104'
124
120p
120o
120c
120b
120a
208
DELAY ELEMENT MODULE
RESET
140
128
TAP 15
TAP 14
TAP 2
TAP 1
TAP 0
200
REFERENCE CLOCK INPUT
STATE CAPTURE MODULE 204'
LAP COUNTER MODULE
SYNCHRONIZATION INPUT
300
220
330
ALGEBRA MODULE 108'
LOOP AVERAGING MODULE 212
SYNCHRONIZATION MODULE 304
SWITCHING MODULE 112
COMPENSATION MODULE 320
FINE DELAY MODULE 310
ARBITRARY WAVEFORM GENERATOR
100'
324
COMPENSATION INPUT
132
ALGEBRA DATA INPUT
OUTPUT MODULE 114
136
OUTPUT SIGNAL

FIG. 4

FIG. 5


FROM STATE CAPTURE MODULE 204'
330
220
128
LOOP AVERAGING MODULE
212
564
568
RISEb
540'
RISE
540
128
SYNCHRONIZATION MODULE 304
CLOCK DOMAIN TRANSFER MODULE 504
592
596
508
512
564
540 RISE
516
568
REGISTER
REGISTER
RISE
540
PERIOD INTEGRATOR MODULE 500
540 RISE
540 RISE
584
540 RISE
560
TO SWITCHING MODULE 112, FINE DELAY MODULE 310, OUTPUT MODULE 114
ALGEBRA DATA INPUT
132
132a
572
REG
520
576
REG
534
580
REGISTER
528
540
REGISTER
RISE
540
532
REGISTER
RISE
536
CONSTANT W
550
USER PHASE MODIFICATION INPUT(REF CLOCKSHIFTING)
132b
PHASE COMPENSATION (TAP SHIFTING)
132c
540
RISE
FROM PHASE COMBINING MODULE 1225
RISEb
540'
ALGEBRA MODULE
108'

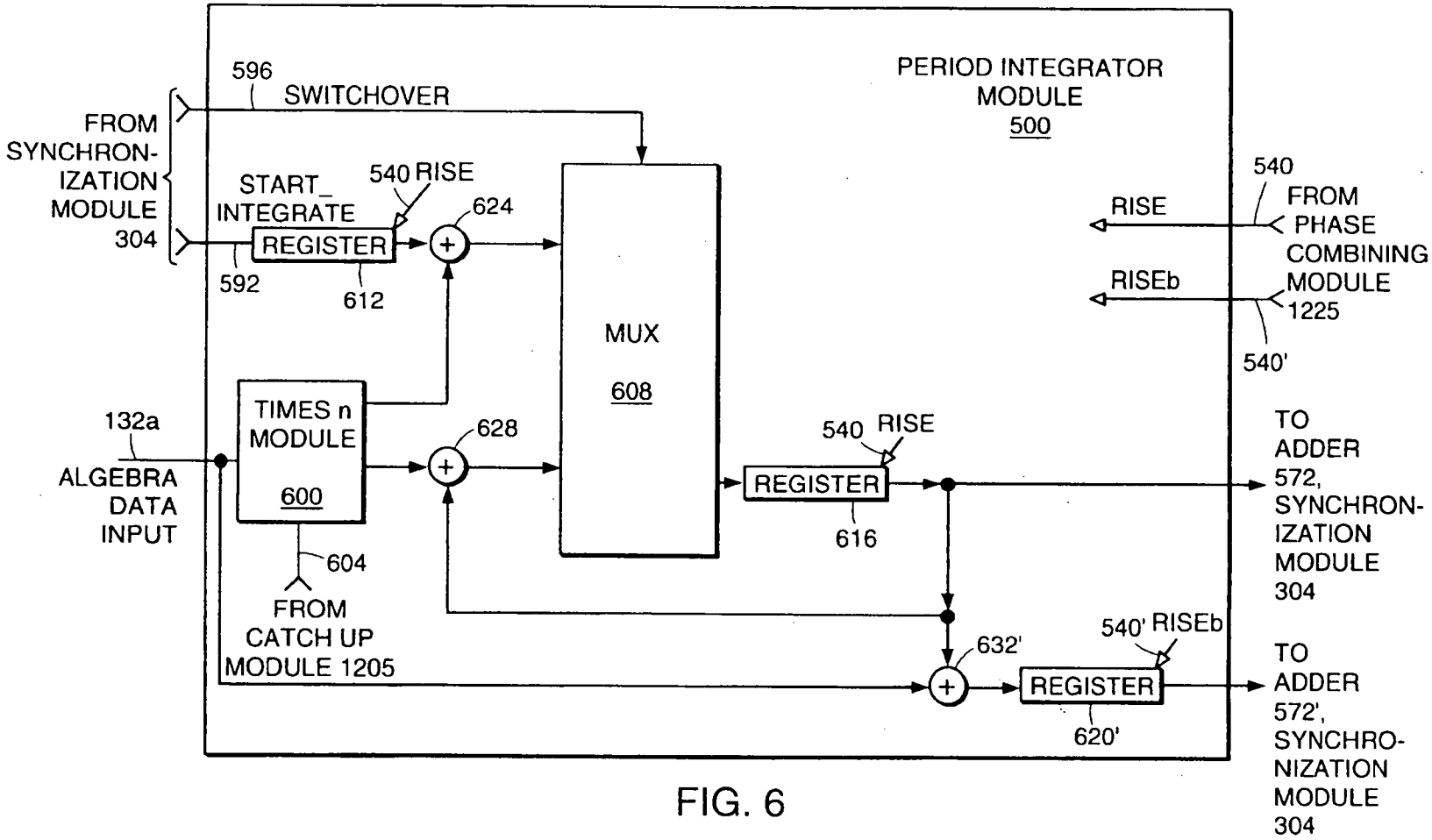

PERIOD INTEGRATOR MODULE 500
596
SWITCHOVER
FROM SYNCHRON-IZATION MODULE 304
START_ INTEGRATE
540 RISE
REGISTER
592
612
624
MUX
608
TIMES n MODULE 600
132a
ALGEBRA DATA INPUT
628
604
FROM CATCH UP MODULE 1205
540 RISE
REGISTER
616
RISE
RISEb
540
FROM PHASE COMBINING MODULE 1225
540'
TO ADDER 572, SYNCHRON-IZATION MODULE 304
632'
540' RISEb
REGISTER
620'
TO ADDER 572', SYNCHRO-NIZATION MODULE 304

FIG. 6

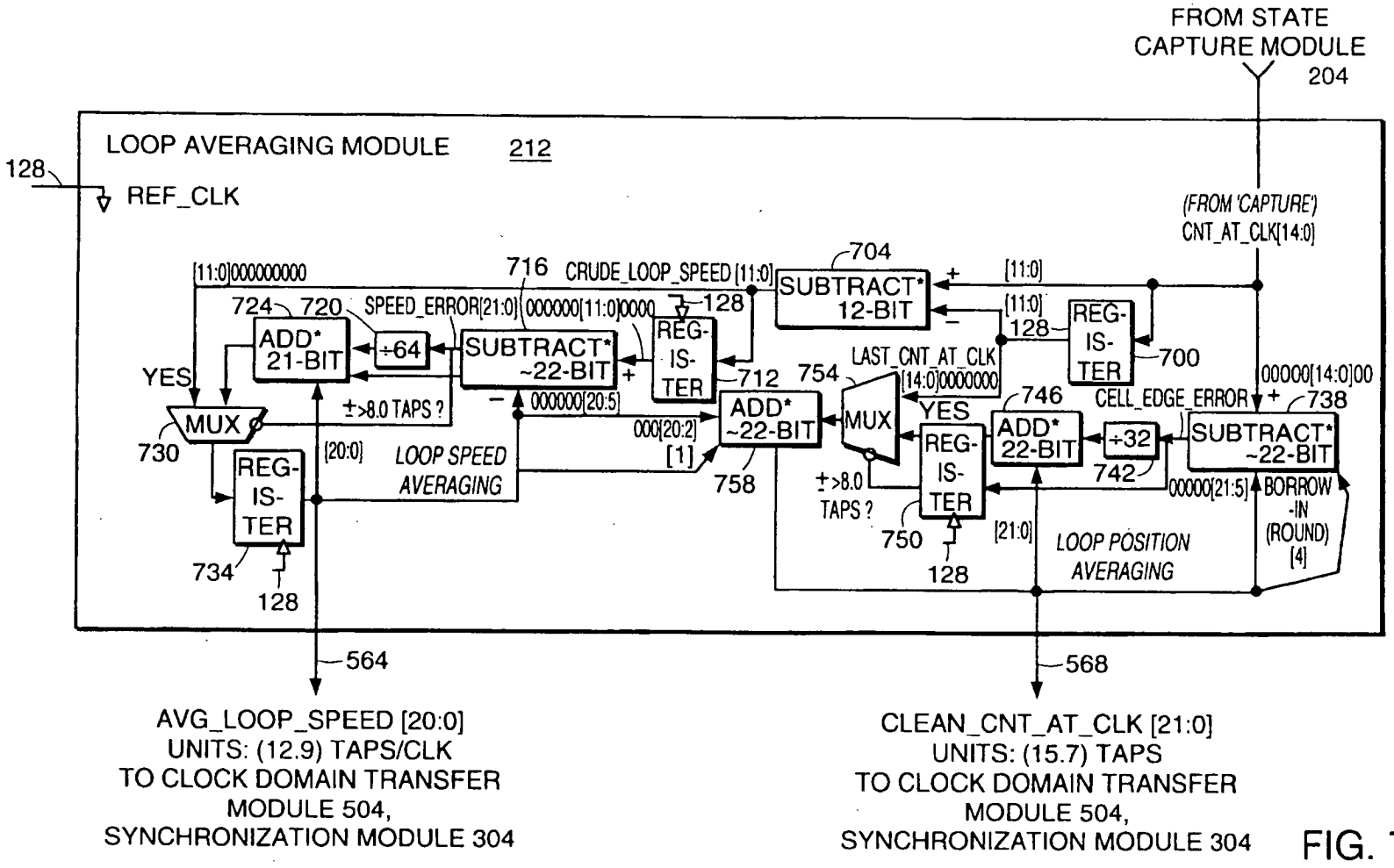

FROM STATE CAPTURE MODULE 204
LOOP AVERAGING MODULE 212
128
REF_CLK
(FROM 'CAPTURE') CNT_AT_CLK[14:0]
[11:0]000000000
716
CRUDE_LOOP_SPEED [11:0]
704
SUBTRACT* 12-BIT
[11:0]
724
720
SPEED_ERROR[21:0]
000000[11:0]0000
128
ADD* 21-BIT
÷64
SUBTRACT* ~22-BIT
REG-IS-TER
712
[11:0]
128
REG-IS-TER
700
LAST_CNT_AT_CLK [14:0]0000000
754
00000[14:0]00
YES
±>8.0 TAPS ?
000000[20:5]
MUX
730
000[20:2]
[1]
ADD* ~22-BIT
758
MUX
YES
746
CELL_EDGE_ERROR
738
ADD* 22-BIT
÷32
SUBTRACT* ~22-BIT
742
[20:0]
LOOP SPEED AVERAGING
REG-IS-TER
±>8.0 TAPS ?
750
00000[21:5]
BORROW -IN (ROUND) [4]
[21:0]
LOOP POSITION AVERAGING
734
128
128
564
568
AVG_LOOP_SPEED [20:0]
UNITS: (12.9) TAPS/CLK
TO CLOCK DOMAIN TRANSFER
MODULE 504,
SYNCHRONIZATION MODULE 304
CLEAN_CNT_AT_CLK [21:0]
UNITS: (15.7) TAPS
TO CLOCK DOMAIN TRANSFER
MODULE 504,
SYNCHRONIZATION MODULE 304

FIG. 7

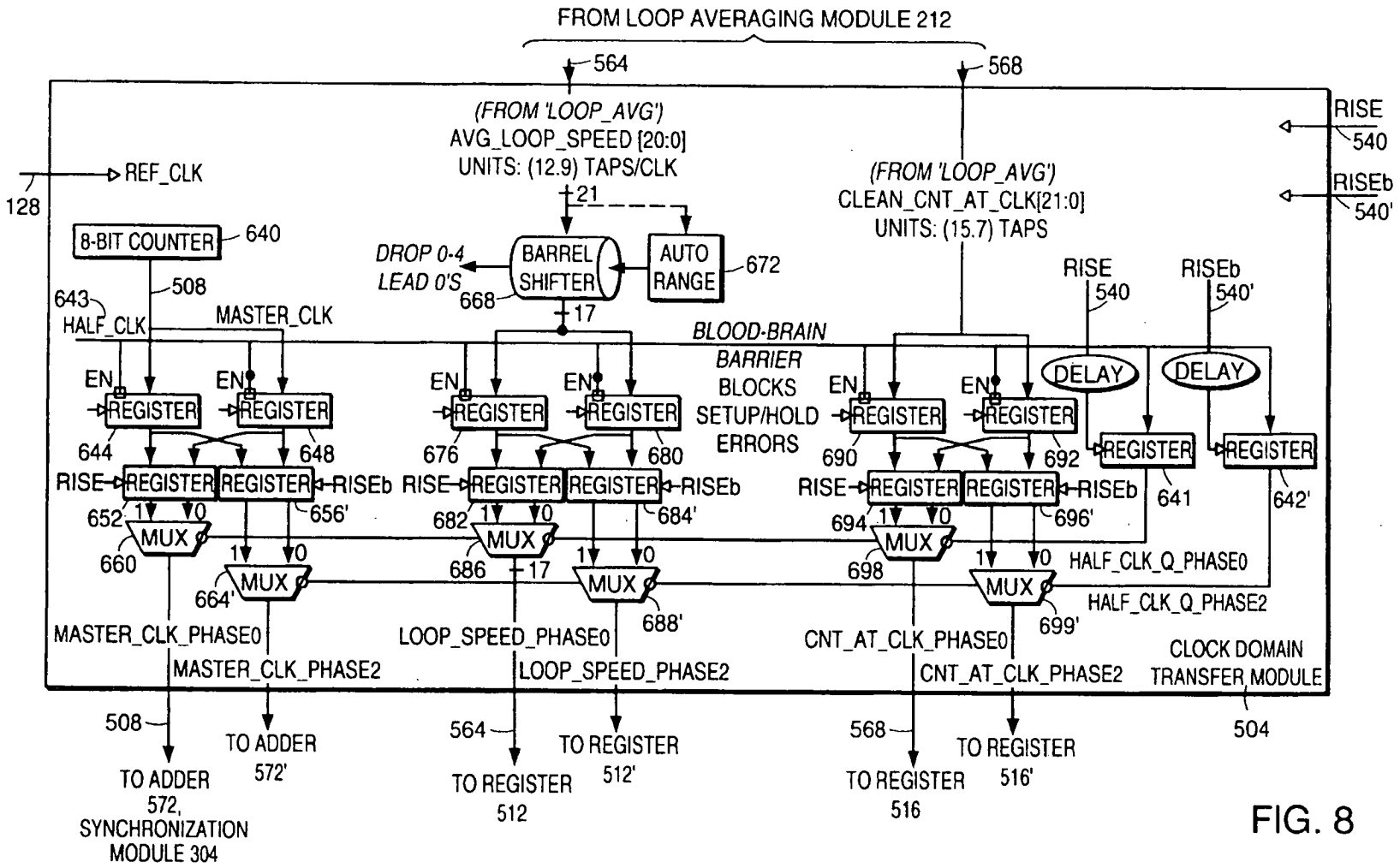

FROM LOOP AVERAGING MODULE 212
564
568
(FROM 'LOOP_AVG')
AVG_LOOP_SPEED [20:0]
UNITS: (12.9) TAPS/CLK
21
(FROM 'LOOP_AVG')
CLEAN_CNT_AT_CLK[21:0]
UNITS: (15.7) TAPS
RISE
540
RISEb
540'
REF_CLK
128
8-BIT COUNTER
640
508
643
HALF_CLK
MASTER_CLK
DROP 0-4
LEAD 0'S
BARREL
SHIFTER
668
AUTO
RANGE
672
17
BLOOD-BRAIN
BARRIER
BLOCKS
SETUP/HOLD
ERRORS
DELAY
REGISTER
644
648
676
680
690
692
641
642'
652
656'
682
684'
694
696'
MUX
660
664'
686
688'
698
699'
HALF_CLK_Q_PHASE0
HALF_CLK_Q_PHASE2
MASTER_CLK_PHASE0
MASTER_CLK_PHASE2
LOOP_SPEED_PHASE0
LOOP_SPEED_PHASE2
CNT_AT_CLK_PHASE0
CNT_AT_CLK_PHASE2
CLOCK DOMAIN
TRANSFER MODULE
504
TO ADDER
572,
SYNCHRONIZATION
MODULE 304
TO ADDER
572'
TO REGISTER
512
TO REGISTER
512'
TO REGISTER
516
TO REGISTER
516'

FIG. 8

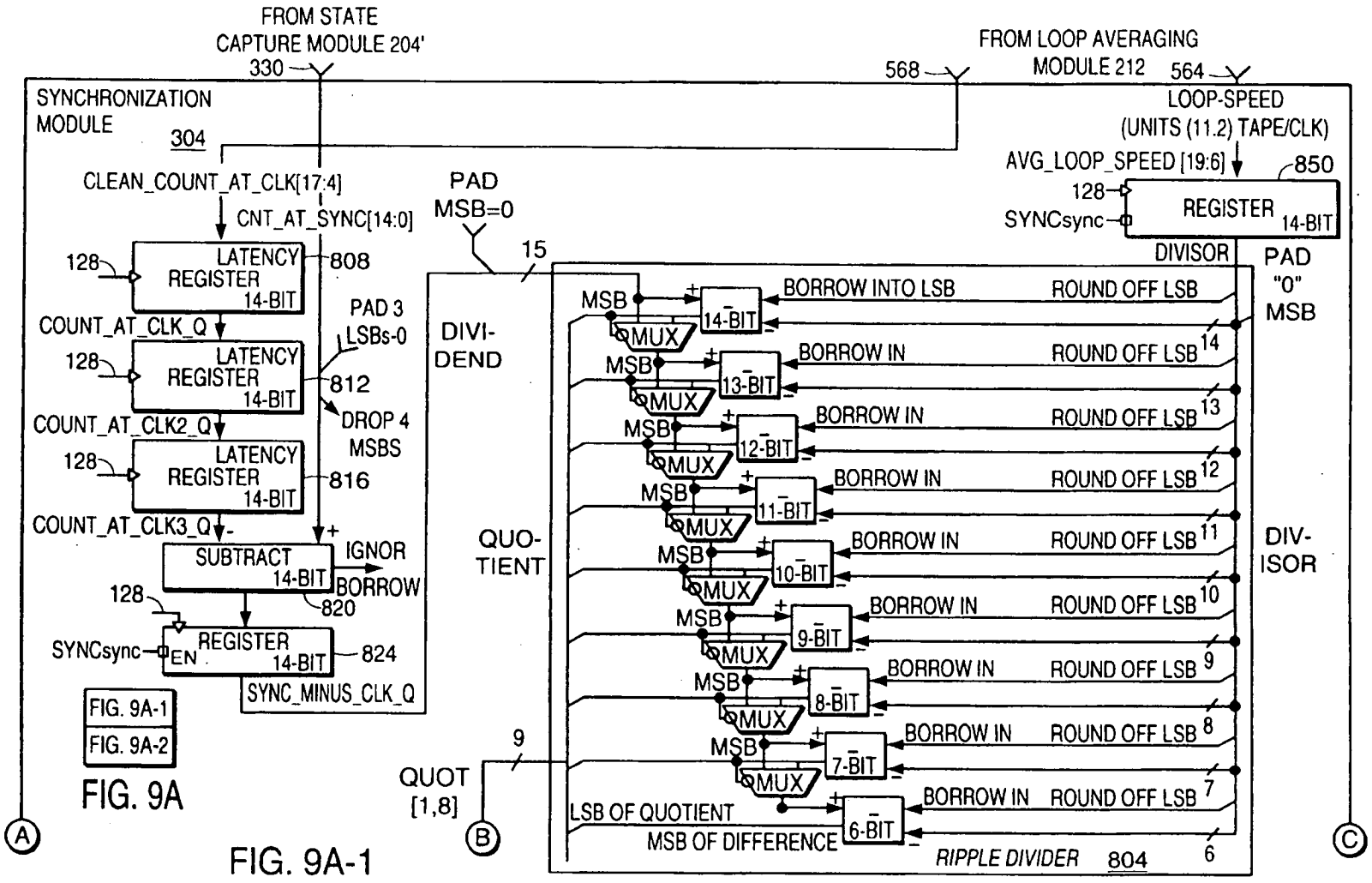


FIG. 9A-1

FIG. 9A-2

FIG. 9A

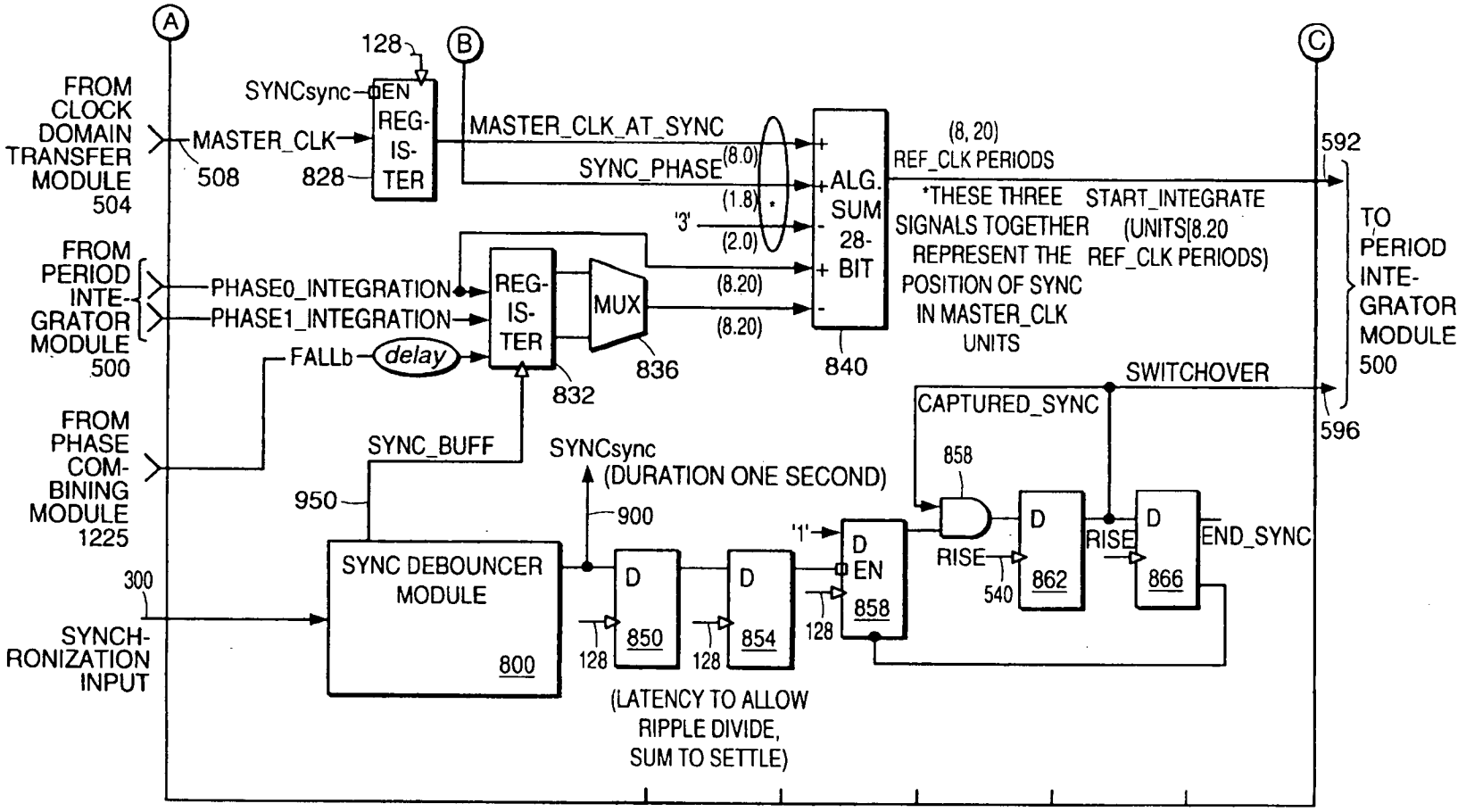

A
B
C
128
FROM CLOCK DOMAIN TRANSFER MODULE 504
SYNCsync
EN
REG-IS-TER
MASTER_CLK
508
828
MASTER_CLK_AT_SYNC
SYNC_PHASE
(8.0)
(1.8)
'3'
(2.0)
ALG. SUM 28-BIT
(8, 20)
REF_CLK PERIODS
*THESE THREE SIGNALS TOGETHER REPRESENT THE POSITION OF SYNC IN MASTER_CLK UNITS
START_INTEGRATE (UNITS[8.20 REF_CLK PERIODS)
592
TO PERIOD INTE-GRATOR MODULE 500
FROM PERIOD INTE-GRATOR MODULE 500
PHASE0_INTEGRATION
PHASE1_INTEGRATION
FALLb
delay
REG-IS-TER
832
MUX
836
(8.20)
(8.20)
840
SWITCHOVER
CAPTURED_SYNC
596
FROM PHASE COM-BINING MODULE 1225
SYNC_BUFF
950
SYNCsync
(DURATION ONE SECOND)
900
858
'1'
D
EN
858
RISE
540
D
862
RISE
D
866
END_SYNC
300
SYNCH-RONIZATION INPUT
SYNC DEBOUNCER MODULE
800
D
850
D
854
128
128
128
(LATENCY TO ALLOW RIPPLE DIVIDE, SUM TO SETTLE)

FIG. 9A-2

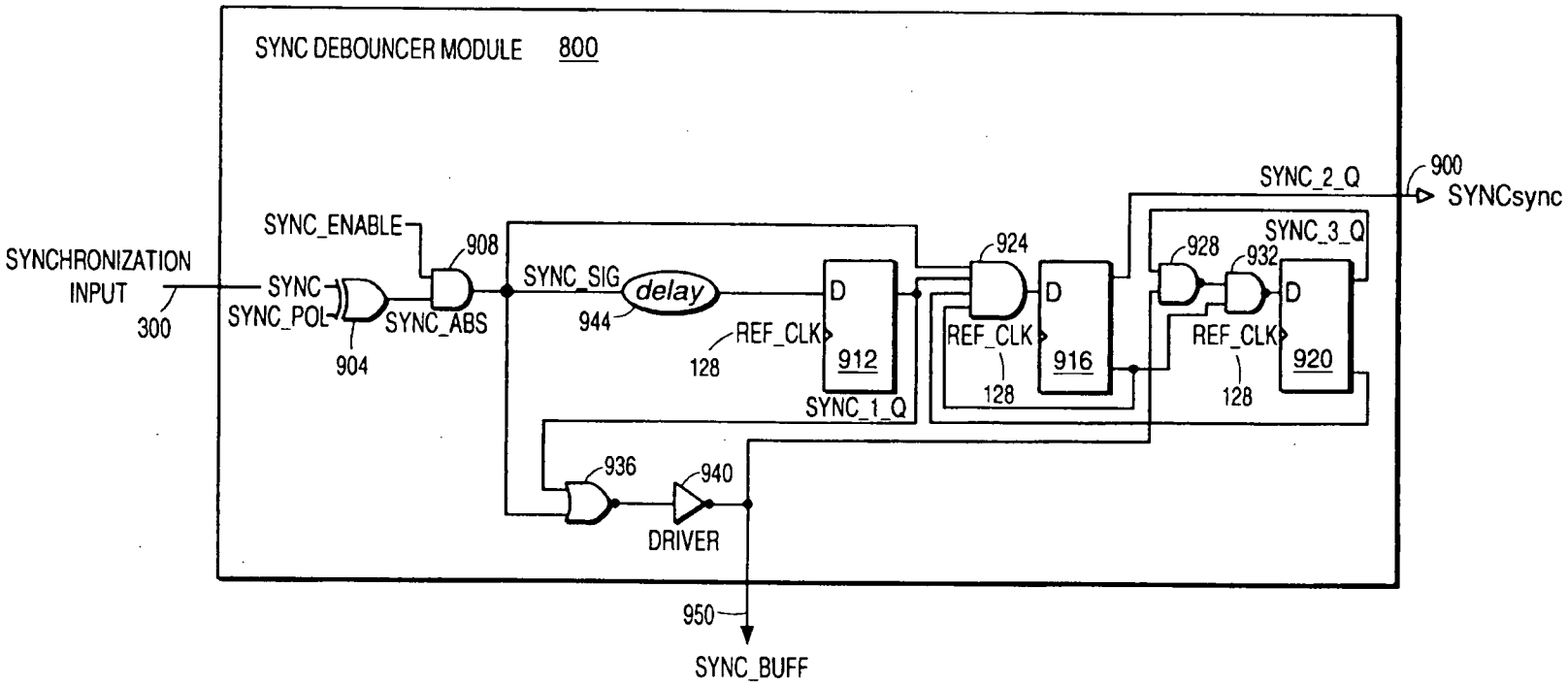

SYNC DEBOUNCER MODULE 800
SYNCHRONIZATION INPUT
300
SYNC
SYNC_POL
904
SYNC_ENABLE
908
SYNC_ABS
SYNC_SIG
944
delay
REF_CLK
128
D
912
SYNC_1_Q
924
D
916
REF_CLK
128
SYNC_2_Q
900
SYNCsync
928
932
SYNC_3_Q
D
920
REF_CLK
128
936
940
DRIVER
950
SYNC_BUFF

FIG. 9B

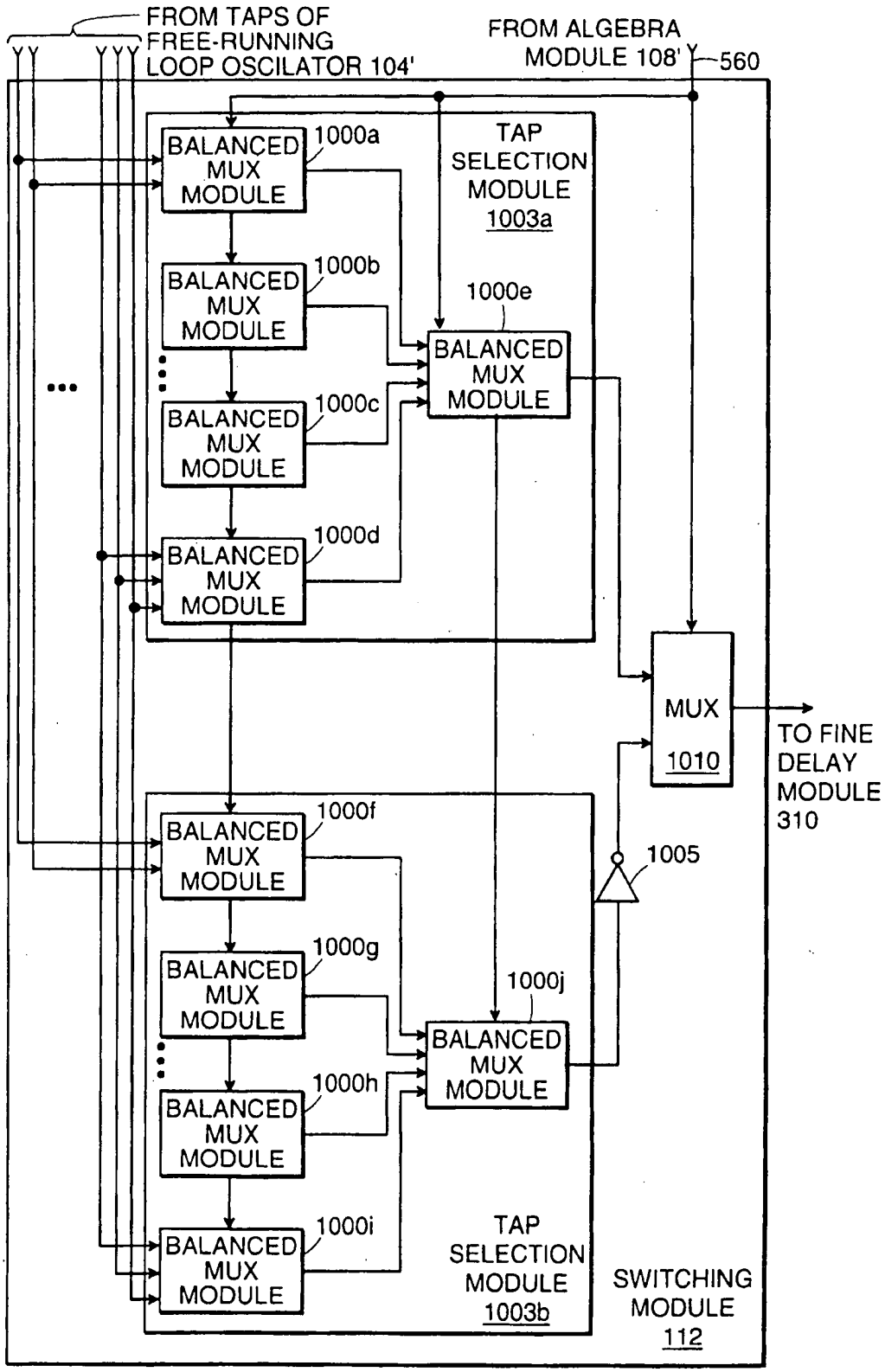

FROM TAPS OF FREE-RUNNING LOOP OSCILATOR 104'
FROM ALGEBRA MODULE 108'
560
BALANCED MUX MODULE
1000a
1000b
1000c
1000d
1000e
1000f
1000g
1000h
1000i
1000j
TAP SELECTION MODULE 1003a
TAP SELECTION MODULE 1003b
MUX 1010
1005
TO FINE DELAY MODULE 310
SWITCHING MODULE 112

FIG. 10A

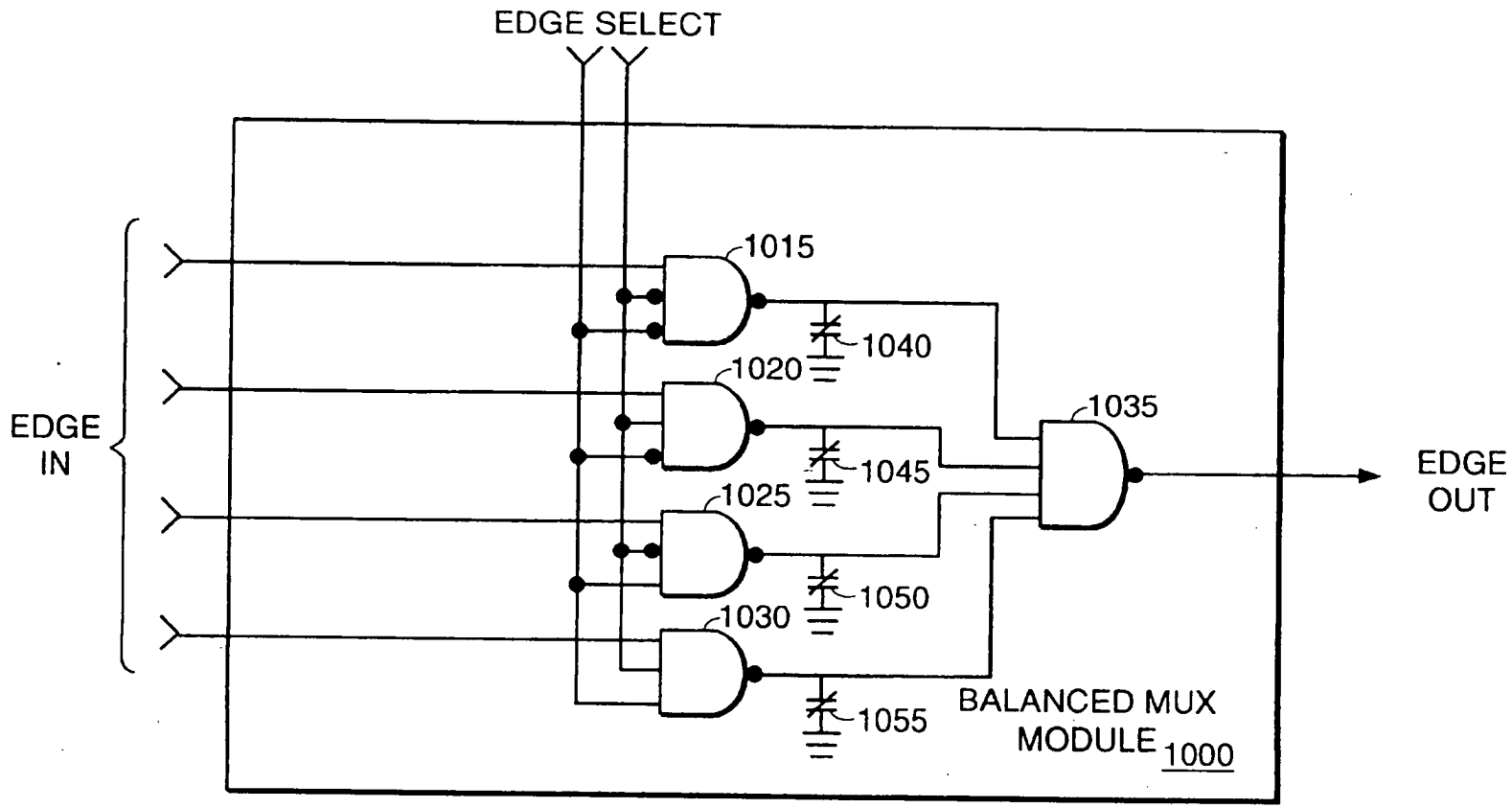

EDGE SELECT
EDGE IN
1015
1040
1020
1045
1035
EDGE OUT
1025
1050
1030
1055
BALANCED MUX MODULE 1000

FIG. 10B

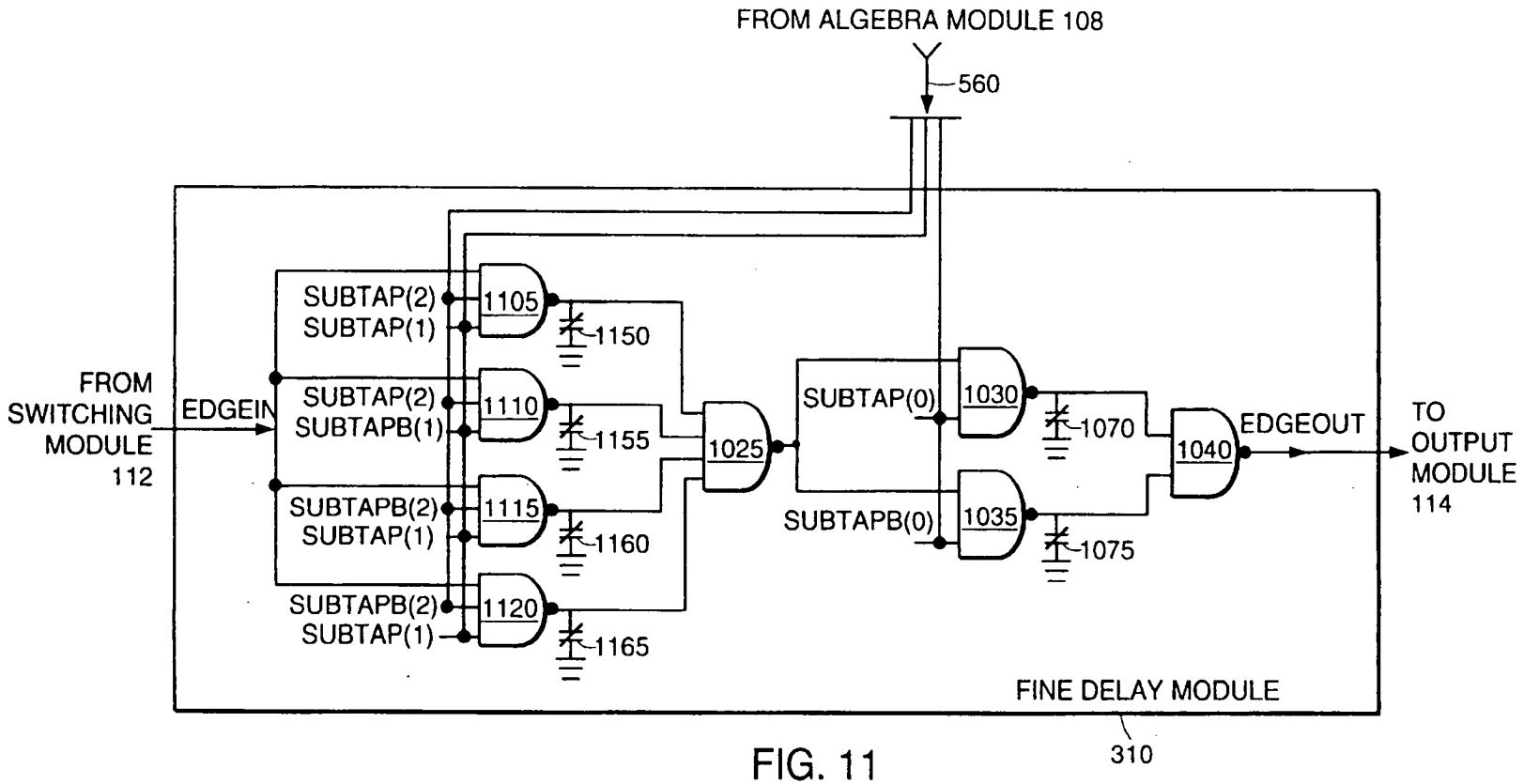

FROM ALGEBRA MODULE 108
560
FROM SWITCHING MODULE 112
EDGEIN
SUBTAP(2)
SUBTAP(1)
1105
1150
SUBTAP(2)
SUBTAPB(1)
1110
1155
SUBTAPB(2)
SUBTAP(1)
1115
1160
SUBTAPB(2)
SUBTAP(1)
1120
1165
1025
SUBTAP(0)
1030
1070
SUBTAPB(0)
1035
1075
1040
EDGEOUT
TO OUTPUT MODULE 114
FINE DELAY MODULE
310

FIG. 11

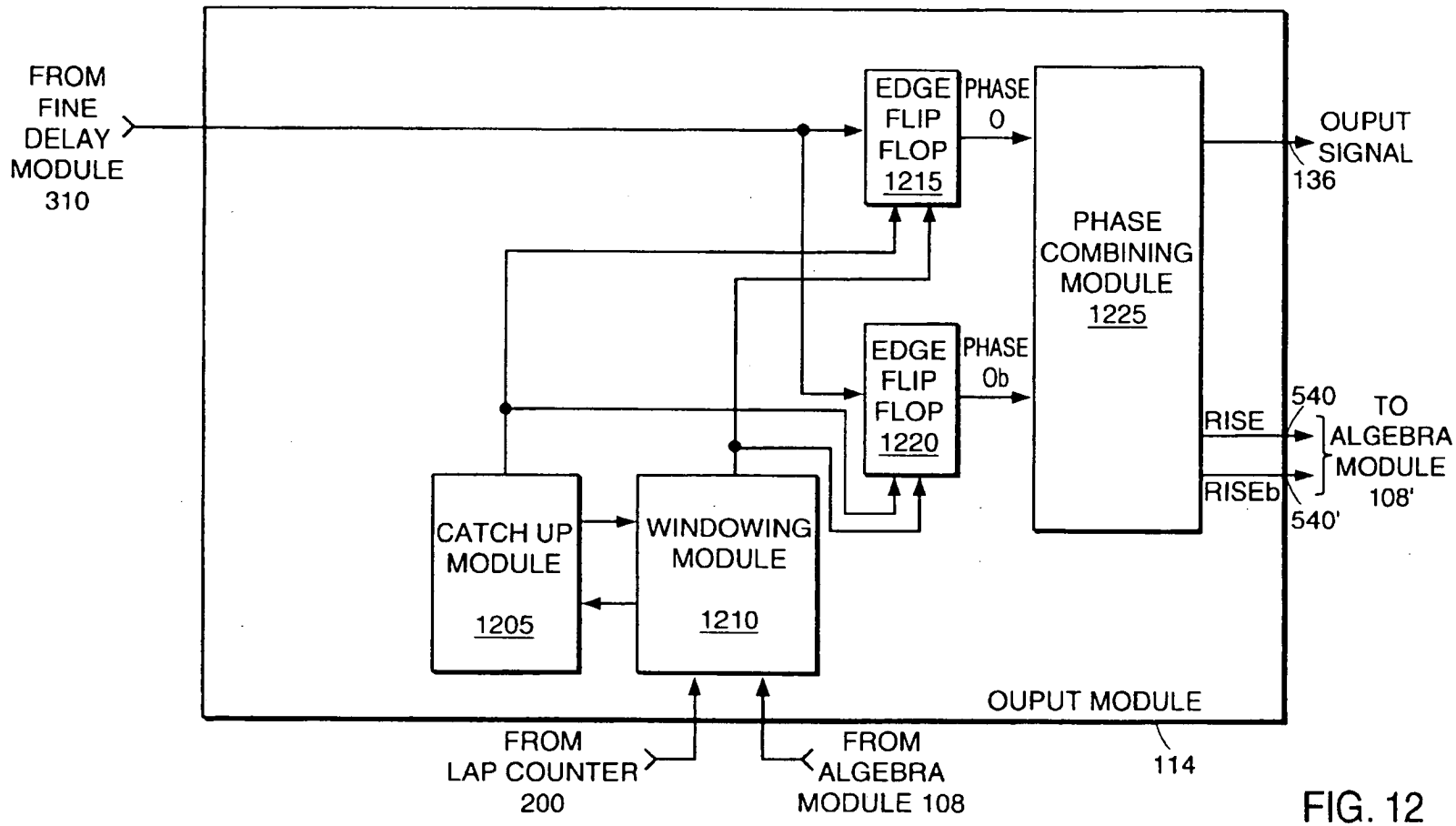

FROM FINE DELAY MODULE 310
EDGE FLIP FLOP 1215
PHASE 0
EDGE FLIP FLOP 1220
PHASE 0b
PHASE COMBINING MODULE 1225
OUPUT SIGNAL 136
RISE
RISEb
540
540'
TO ALGEBRA MODULE 108'
CATCH UP MODULE 1205
WINDOWING MODULE 1210
OUPUT MODULE
114
FROM LAP COUNTER 200
FROM ALGEBRA MODULE 108

FIG. 12

FIG. 13A	FIG. 13B

FIG. 13

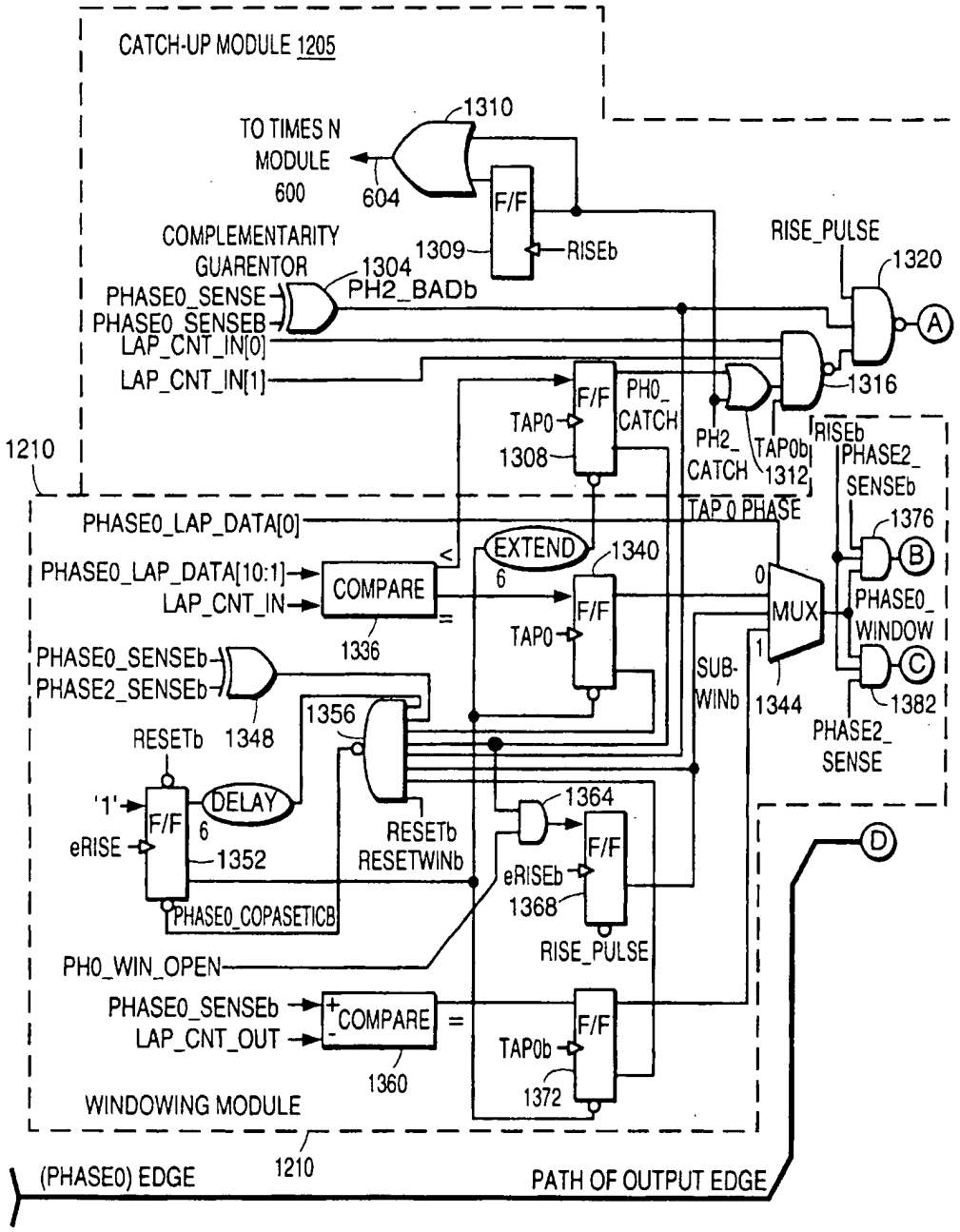


FIG. 13A

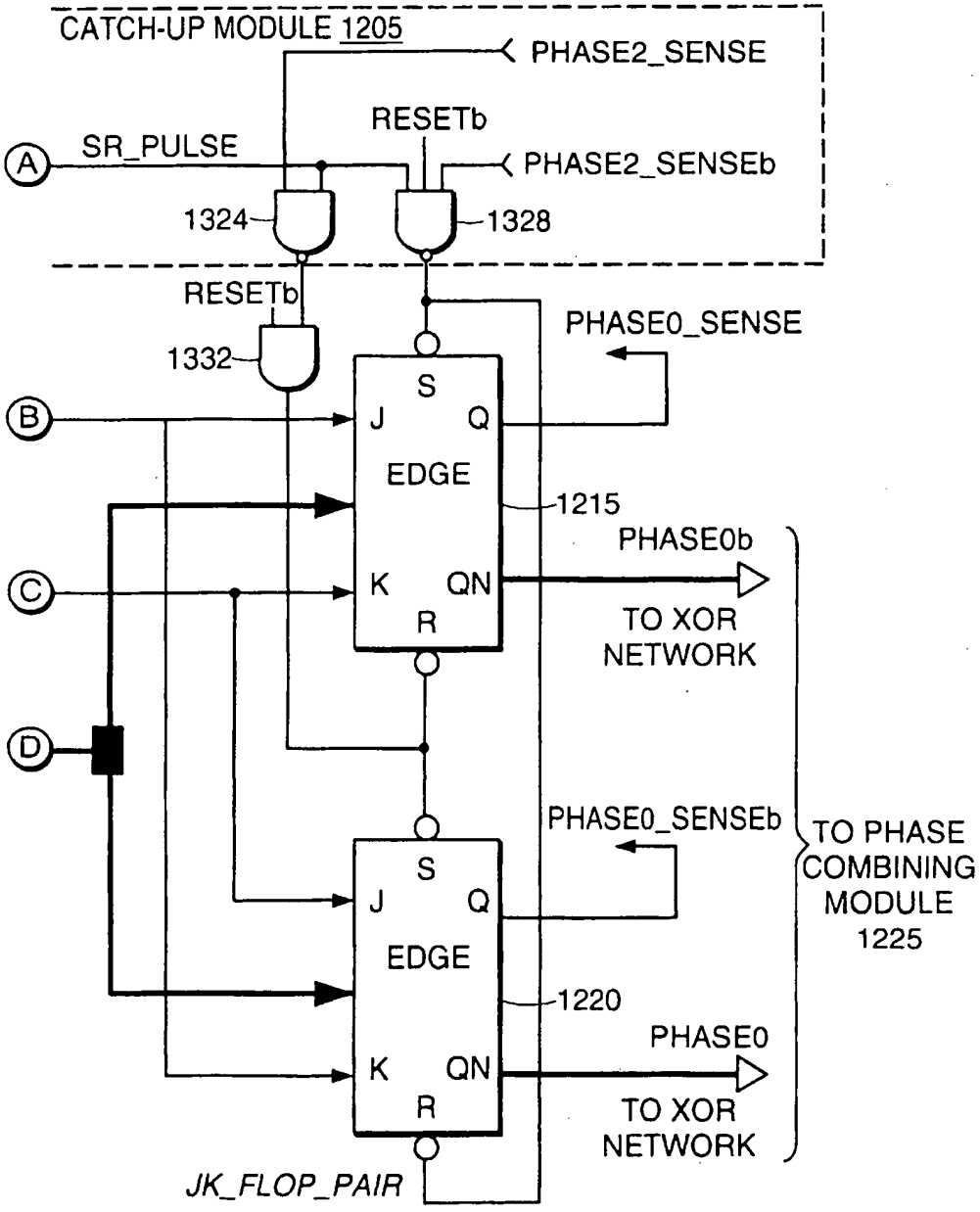

CATCH-UP MODULE 1205
PHASE2_SENSE
RESETb
SR_PULSE
A
PHASE2_SENSEb
1324
1328
RESETb
1332
PHASE0_SENSE
B
S
J
Q
EDGE
1215
PHASE0b
C
K
QN
R
TO XOR NETWORK
D
PHASE0_SENSEb
TO PHASE COMBINING MODULE 1225
S
J
Q
EDGE
1220
PHASE0
K
QN
R
TO XOR NETWORK
JK_FLOP_PAIR

FIG. 13B

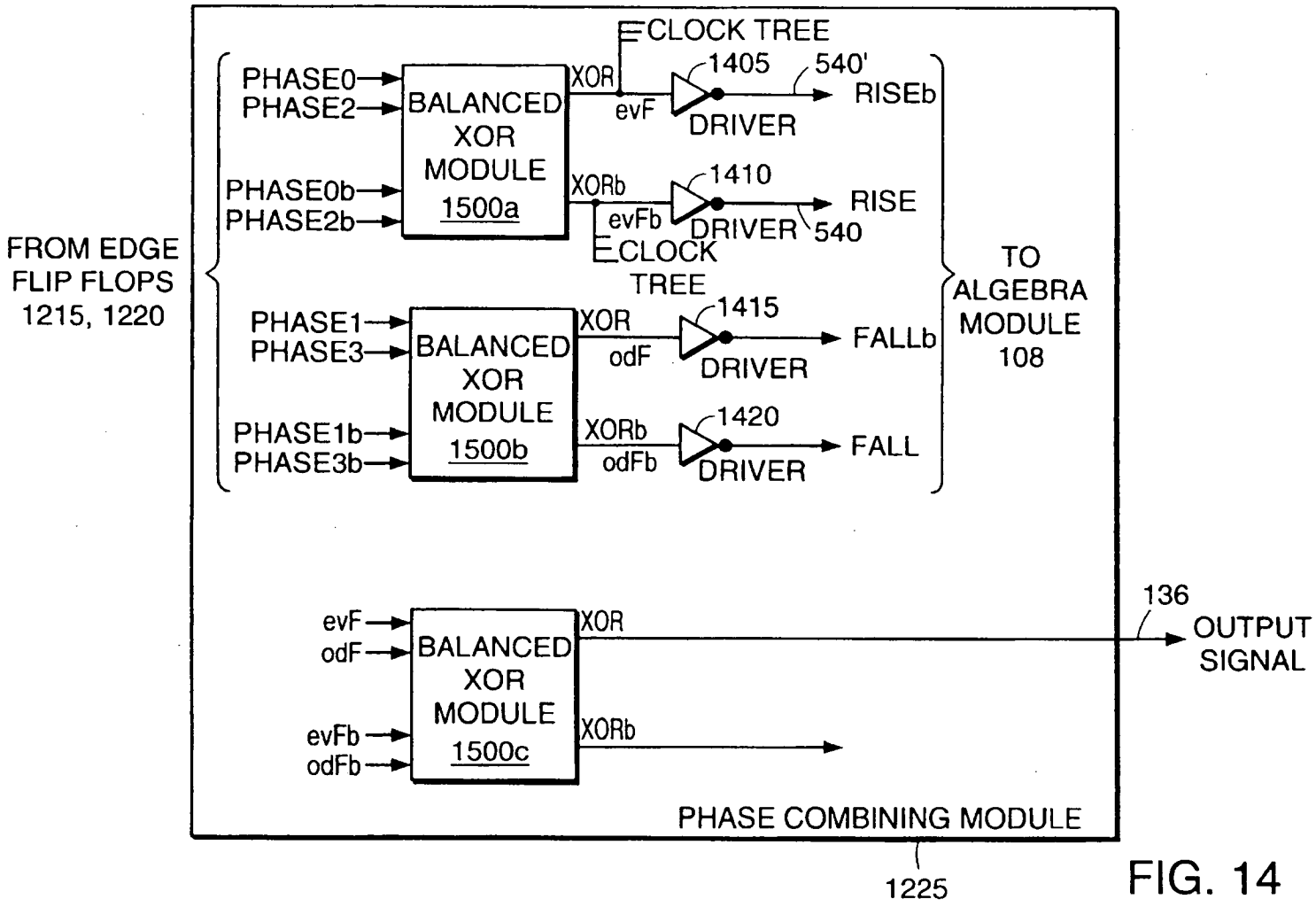

FROM EDGE FLIP FLOPS 1215, 1220
PHASE0
PHASE2
PHASE0b
PHASE2b
BALANCED XOR MODULE 1500a
XOR
XORb
evF
evFb
CLOCK TREE
1405
1410
DRIVER
DRIVER
540'
540
RISEb
RISE
CLOCK TREE
PHASE1
PHASE3
PHASE1b
PHASE3b
BALANCED XOR MODULE 1500b
XOR
XORb
odF
odFb
1415
1420
DRIVER
DRIVER
FALLb
FALL
TO ALGEBRA MODULE 108
evF
odF
evFb
odFb
BALANCED XOR MODULE 1500c
XOR
XORb
136
OUTPUT SIGNAL
PHASE COMBINING MODULE
1225

FIG. 14

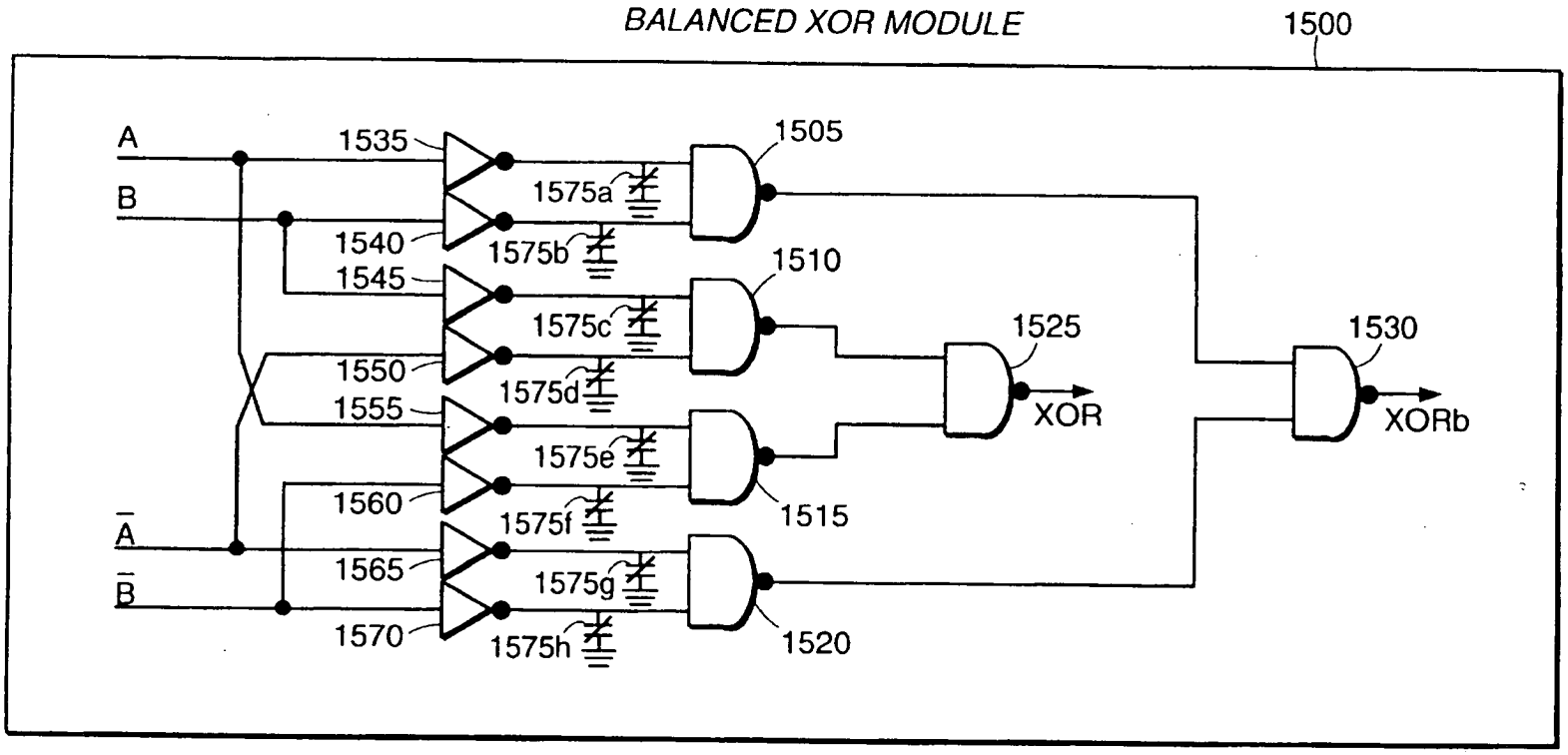

BALANCED XOR MODULE
1500
A
B
$\bar{A}$
$\bar{B}$
1535
1540
1545
1550
1555
1560
1565
1570
1575a
1575b
1575c
1575d
1575e
1575f
1575g
1575h
1505
1510
1515
1520
1525
1530
XOR
XORb

FIG. 15

OUTPUT PERIOD ILLUSTRATED: 7NS [143 MHz]
WORST CASE PROPAGATIONS SHOWN

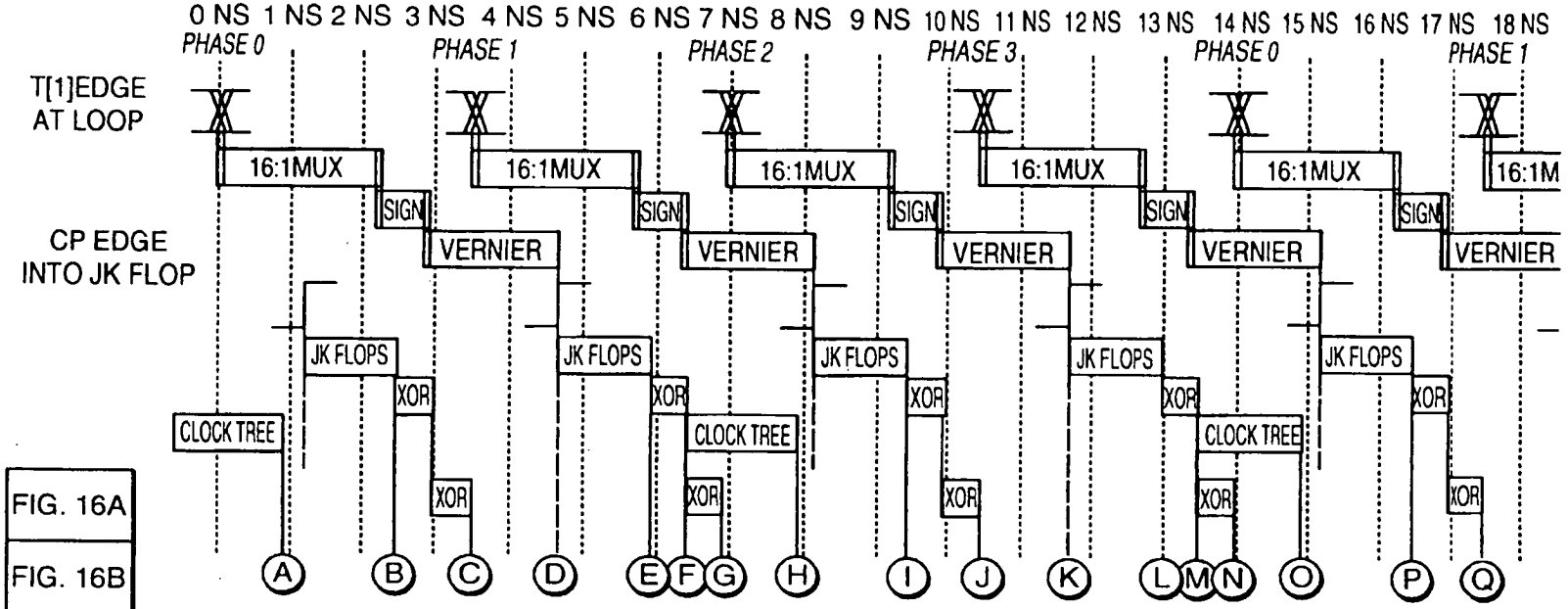


FIG. 16A

FIG. 16A
FIG. 16B
FIG. 16C
FIG. 16D

FIG. 16

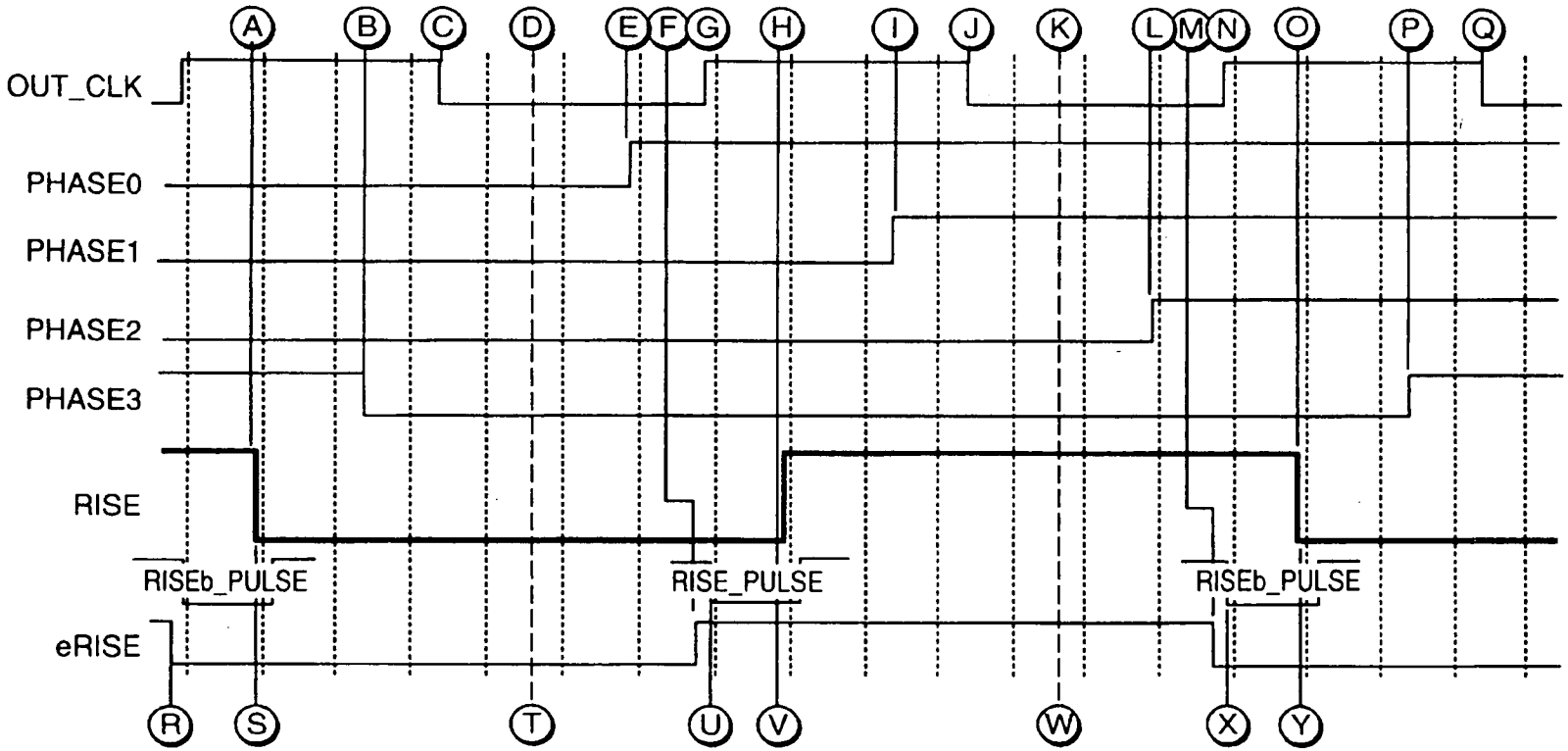
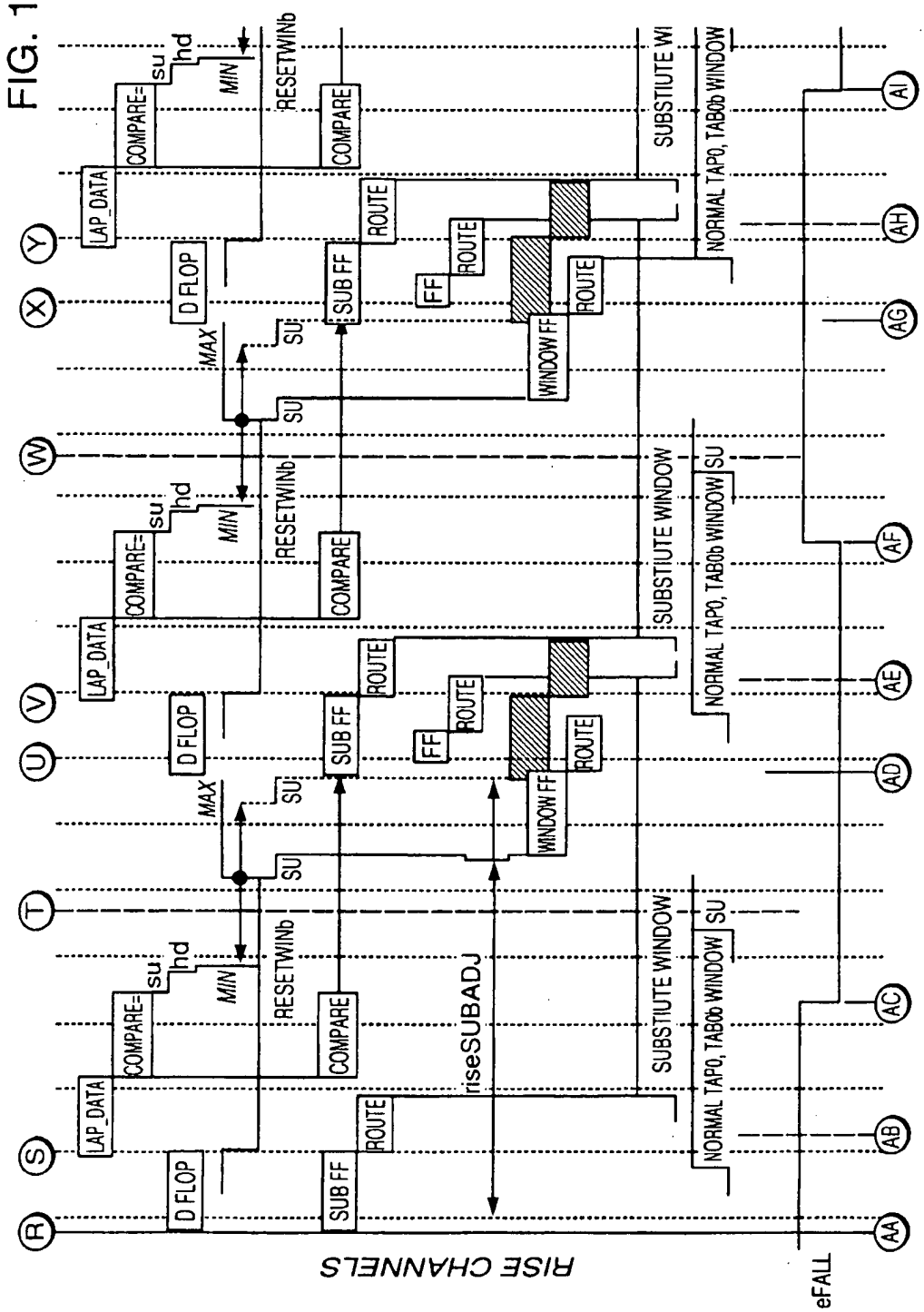

A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
OUT_CLK
PHASE0
PHASE1
PHASE2
PHASE3
RISE
RISEb_PULSE
RISE_PULSE
RISEb_PULSE
eRISE
R
S
T
U
V
W
X
Y

FIG. 16B

FIG. 16C


RISE CHANNELS
eFALL
R
S
T
U
V
W
X
Y
AA
AB
AC
AD
AE
AF
AG
AH
AI
LAP_DATA
COMPARE=
su
hd
MIN
RESETWINb
COMPARE
D FLOP
SUB FF
ROUTE
FF
WINDOW FF
MAX
SU
riseSUBADJ
SUBSTIUTE WINDOW
NORMAL TAP0, TAB0b WINDOW

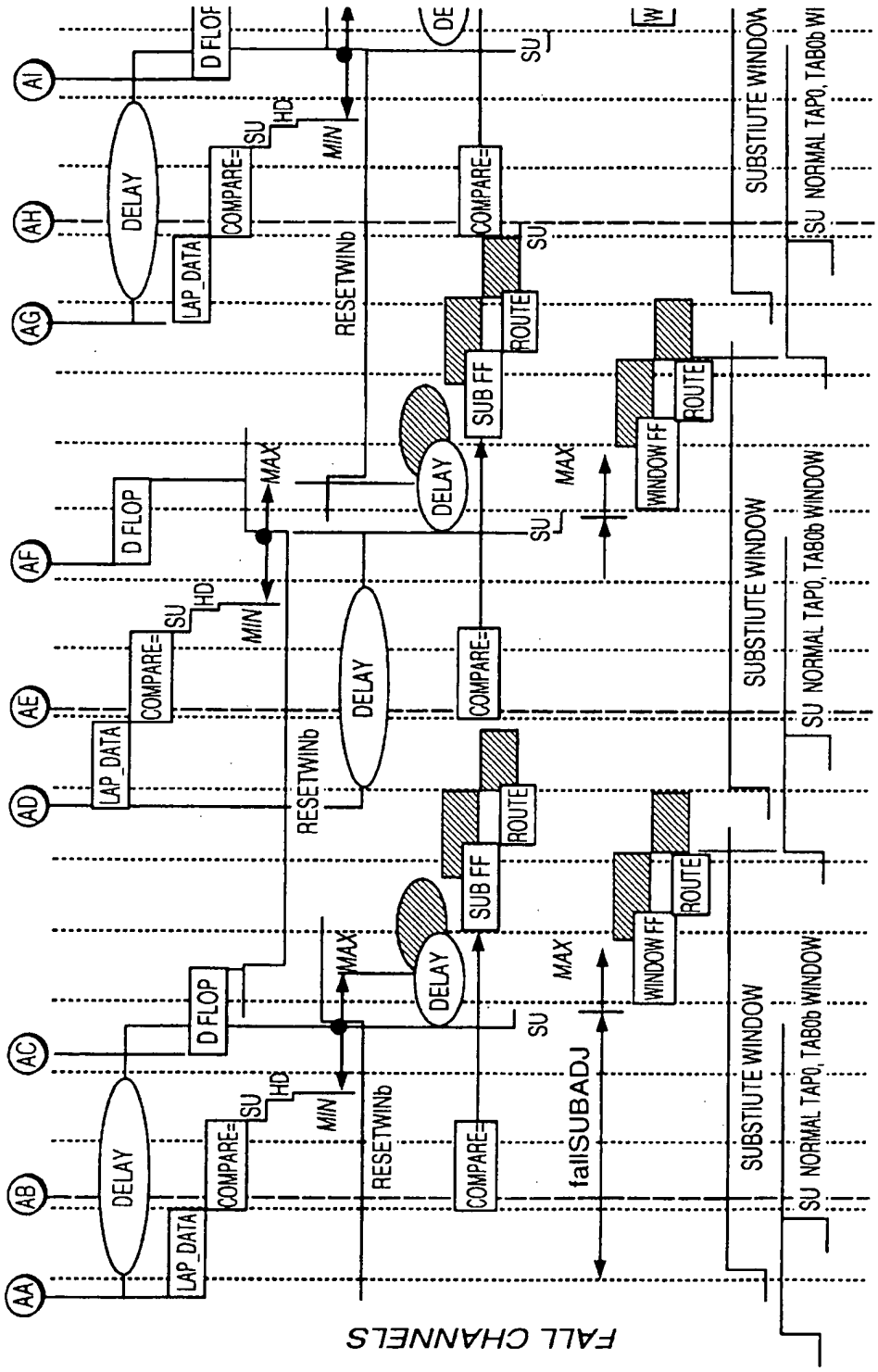

FALL CHANNELS
AA
AB
AC
AD
AE
AF
AG
AH
AI
DELAY
LAP_DATA
COMPARE=
SU
HD
MIN
D FLOP
RESETWINb
MAX
SUB FF
ROUTE
WINDOW FF
SUBSTIUTE WINDOW
SU NORMAL TAP0, TAB0b WINDOW
fallSUBADJ

FIG. 16D